

WHAT IS CLAIMED IS:

1                   1.       A mask for manufacturing integrated circuits, the mask comprising:  
2                   a mask substrate;  
3                   an active mask region within a first portion of the mask substrate, the active  
4 region being adapted to accumulate a pre-determined level of static electricity;  
5                   a first guard ring structure surrounding a portion of the active mask region to  
6 isolate the active region from an outer region of the mask substrate; and  
7                   a second guard ring structure having at least one fuse structure surrounding a  
8 portion of the first guard ring structure;  
9                   wherein the fuse structure is operably coupled to the active region to absorb a  
10 current from static electricity, the static electricity being accumulated by the active region to  
11 the pre-determined level and being discharged as current to the fuse structure while  
12 maintaining the active region free from damage from the static electricity.

1                   2.       The mask of claim 1 wherein the fuse structure is a plurality of  
2 conductive regions.

1                   3.       The mask of claim 1 wherein the fuse structure has a length and a  
2 thickness.

1                   4.       The mask of claim 1 wherein the fuse structure is made of a conductive  
2 material.

1                   5.       The mask of claim 1 wherein each of the fuse structures is formed on  
2 the mask substrate within a predetermined distance from a portion of the active region such  
3 that static electricity discharges to the fuse structure.

1                   6.       The mask of claim 1 wherein the fuse structure includes a plurality of  
2 conductive members, each of the conductive members including an elongated portion  
3 including a free end portion.

1                   7.       The mask of claim 1 wherein the first guard ring structure comprises a  
2 trench region free from an overlying conductive layer.

1                   8.       The mask of claim 1 wherein the first guard ring structure is  
2 continuous around the active region to electrically and physically isolate the second guard  
3 ring structure from the active region.

1                   9.       The mask of claim 1 wherein the predetermined level corresponds to a  
2 voltage no greater than 2,000,000 volts.

1                   10.      The mask of claim 1 wherein the predetermined level corresponds to a  
2 voltage no greater than 2,000,000 volts.

1                   11.      A method for manufacturing a semiconductor integrated circuit device  
2 structure comprising:

3                   using a mask substrate, the mask substrate comprising:

4                   an active mask region within a first portion of the mask substrate, the  
5 active region being adapted to accumulate a pre-determined level of static electricity;

6                   a first guard ring structure surrounding a portion of the active mask  
7 region to isolate the active region from an outer region of the mask substrate; and

8                   a second guard ring structure having at least one fuse structure  
9 surrounding a portion of the first guard ring structure; the fuse structure being  
10 operably coupled to the active region to absorb a current from static electricity, the  
11 static electricity being accumulated by the active region to the pre-determined level  
12 and being discharged as current to the fuse structure while maintaining the active  
13 region free from damage from the static electricity.

1                   12.      The method of claim 11 wherein the fuse structure is a plurality of  
2 conductive regions.

1                   13.      The method of claim 11 wherein the fuse structures is formed on the  
2 mask substrate within a predetermined distance from a portion of the active region such that  
3 static electricity discharges to the fuse structure.

1                   14.      The method of claim 11 the first guard ring structure is continuous  
2 around the active region to electrically and physically isolate the second guard ring structure  
3 from the active region.

1                    15.     The method of claim 11 wherein the fuse structure includes a plurality  
2 of conductive members, each of the conductive members including an elongated portion  
3 including a free end portion.

1                    16.     The method of claim 11 wherein each of the fuse structures is formed  
2 on the mask substrate within a predetermined distance from a portion of the active region  
3 such that static electricity discharges to the fuse structure.

1                    17.     A method for manufacturing integrated circuit devices, the method  
2 comprising:  
3                    receiving a mask in a first pod, the mask including an active region and a  
4 guard ring structure having at least one fuse structure;  
5                    transferring the mask from the first pod into a second pod within a clean room  
6 environment;  
7                    handling the mask in the clean room environment;  
8                    accumulating static electricity on the mask during the handling in the clean  
9 room environment;  
10                    discharging a portion of the static charge to the fuse on the guard ring structure  
11 of the mask while maintaining the active region of the mask free from static energy damage;  
12 and  
13                    using the mask in an operation for manufacture of semiconductor integrated  
14 circuits.

1                    18.     The method of claim 17 wherein the operation is a lithography process.

1                    19.     The method of claim 17 wherein the static energy is characterized by a  
2 voltage of 1000 volts.

1                    20.     The method of claim 17 wherein the static energy is characterized by a  
2 voltage of greater than 3000 volts.